500KHz, 18V/2A &3A Synchronous Step-Down Converter

FEATURES

- High Efficiency: Up to 94%(@3.3V)
- 500KHz Frequency Operation
- 2A&3A Output Current
- No Schottky Diode Required
- 4.5V to 18V Input Voltage Range
- Output Adjustable Down to 0.923V
- Slope Compensated Current Mode Control for Excellent Line and Load Transient Response
- Integrated internal compensation
- Stable with Low ESR Ceramic Output Capacitors
- Over Current Protection
- Thermal Shutdown
- Inrush Current Limit and Soft Start

GENERAL DESCRIPTION

The STI348X is a fully integrated, high–efficiency 2A&3A synchronous rectified step-down converter. The STI348X operates at high efficiency over a wide output current load range.

This device offers two operation modes, PWM control and PFM Mode switching control, which allows a high efficiency over the wider range of the load.

The STI348X requires a minimum number of readily available standard external components and is available in an 8-pin SOP ROHS compliant package

APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors Digital
- Wireless and DSL Modems

TYPICAL APPILCATION

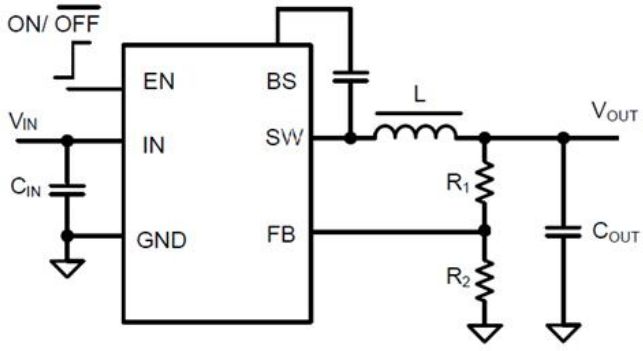
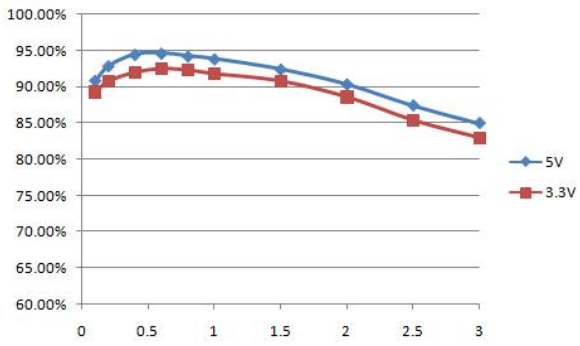


Figure 1. Basic Application CircuitFigure

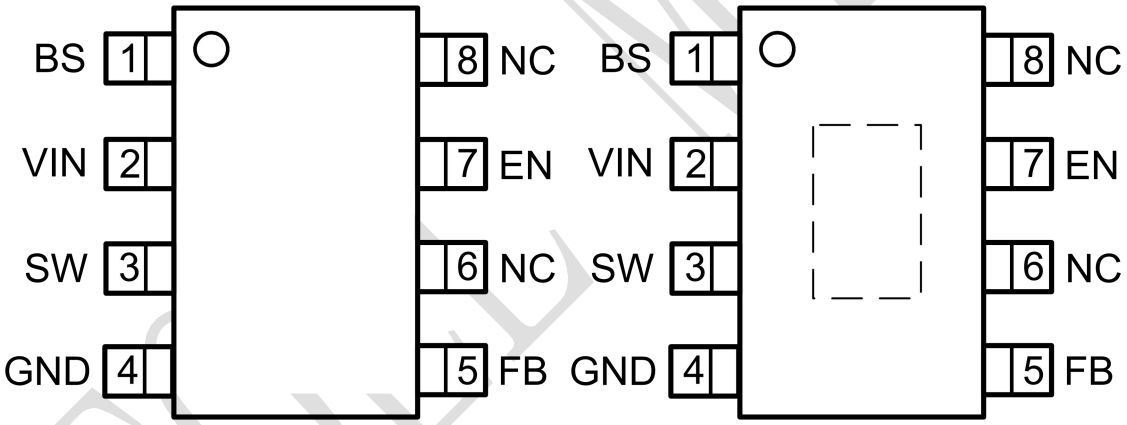


2. Efficiency(%) vs. Load Current(mA)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Value	Unit
Input Supply Voltage ,EN	-0.3~21V	V
SW Voltages	-0.3~Vin+0.3	V
FB Voltage	-0.3~6	V
BS Voltage	Vin-0.3~ Vin+0.3	V
Storage Temperature Range	-65~150	°C
Junction Temperature(Note2)	155	°C
Lead Temperature(Soldering,10s)	260	°C

PACKAGE/ORDER INFORMATION



SOP8
STI3482

ESOP8
STI3484

Top Mark: S3482 YY XXX or S3484 YY XXX

Part Number	Package	Top mark	Quantity/ Reel
STI3482	SOP8	S3482 YY XXX	3000
STI3484	ESOP8	S3484 YY XXX	3000

PIN FUNCTIONS

Pin	Name	Function
1	BS	Bootstrap. A capacitor connected between SW and BS pins is required to form a floating supply across the high-side switch driver.
2	VIN	Power supply Pin
3	SW	Switching Pin
4	GND	Ground
5	FB	Adjustable version feedback input. Connect FB to the center point of the external resistor divider.
6	NC	No Connect
7	EN	Enable Pin. EN is pulled up to 3V with a 1uA current, and contains a precise 1.4V logic threshold. Drive this pin to a logic-high or leave unconnected to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode.
8	NC	No Connect

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human Body Model for all pins	±2000	V

JEDEC specification JS-001

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
Voltage Range	IN	4.5	18	V
TA	Operating Temperature Range	-40	85	°C

ELECTRICAL CHARACTERISTICS (Note 3)

(V_{IN}=12V ,V_{OUT}=3.3V , T_A = 25°C, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.5		18	V
UVLO Threshold			3.5	4.5	V
Quiescent Current	V_{EN}=2.0V, I_{OUT}=0， V_{FB}=V_{REF}*105%		400	600	uA
Shutdown Current	EN =0		4	8	uA
Regulated Feedback Voltage	T_A = 25°C, 4.5V≤V_{IN} ≤18V	0.905	0.923	0.940	V
High-Side Switch On-Resistance	STI3482		110		m Ω
	STI3484		110		m Ω
Low-Side Switch On-Resistance	STI3482		70		m Ω
	STI3484		70		m Ω
High-Side Switch Leakage Current	V_{EN}=0V, V_{SW}=0V		0	10	uA
Upper Switch Current Limit	STI3482		3		A
	STI3484		4		A
Oscillation Frequency	V_{FB}=0.923V		0.5		MHz
Maximum Duty Cycle			95		%
Minimum On-Time			60		nS
Thermal Shutdown			160		℃

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + (P_D)$ x (250°C/W).

Note 3: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency

OPERATION

Internal Regulator

The STI348X is a current mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 500KHz operating frequency to ensure a compact, high efficiency design with excellent AC and DC performance.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal FB reference (VFB) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.923V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally fixed to 1.5 ms.

Over-Current-Protection and Hiccup

The STI348X has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a UV is triggered, the STI348X enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-short to ground. The average short circuit current is greatly reduced to alleviate the thermal issue and to protect the regulator. The STI348X exits the hiccup mode once the over current condition is removed.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The

COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

FUNCTIONAL BLOCK DIAGRAM

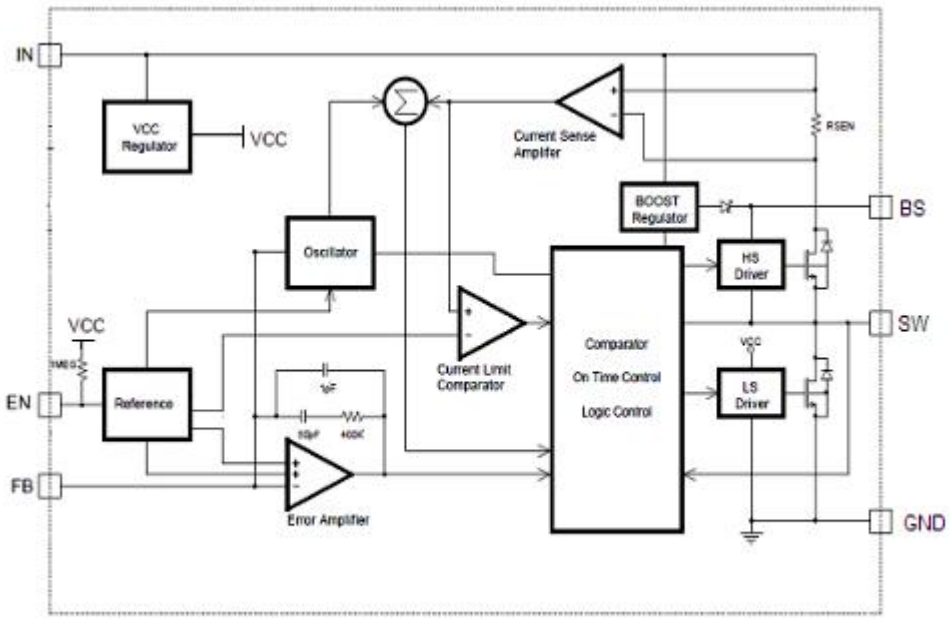
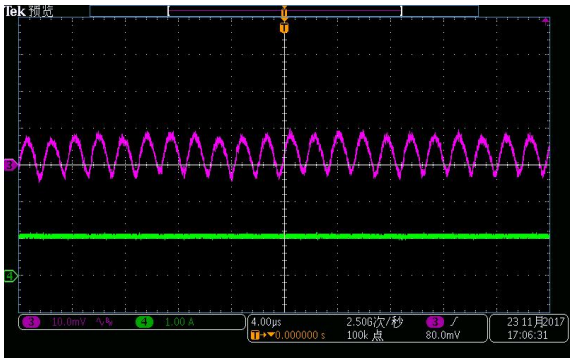


Figure 3. STI3482/4 Block Diagram

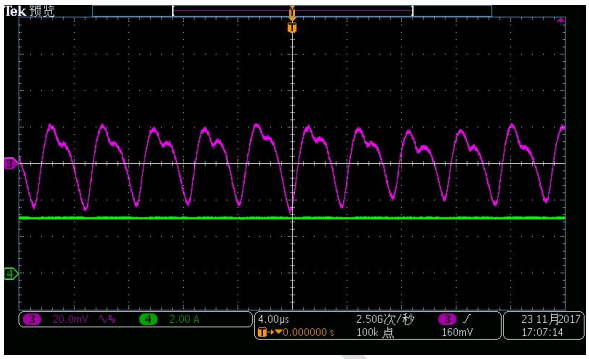
FUNCTIONAL TEST

1.Vout ripple

CH3:VOUT(AC);CH4:Iout



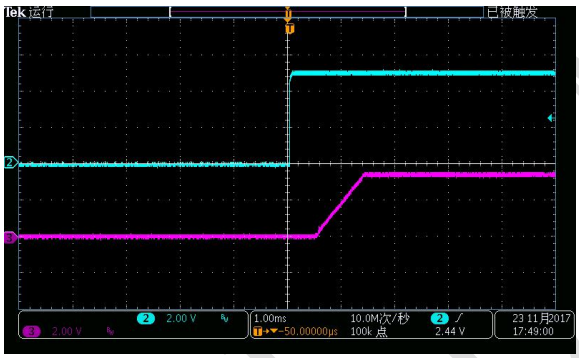
CH3:VOUT(AC);CH4:Iout



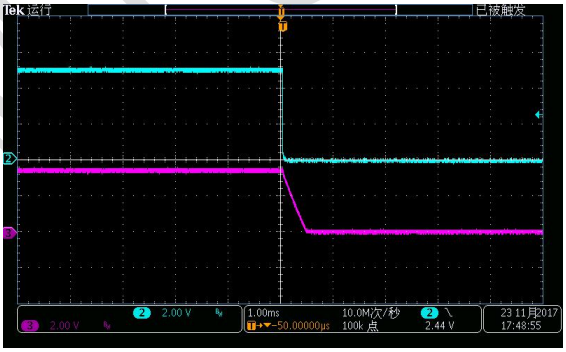
Iout=50% load Iout=100% load

2.Power on/off:

CH2:EN;CH3:VOUT



CH2:EN;CH3:VOUT

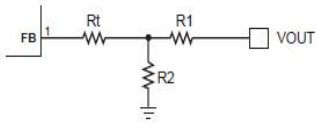


APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Typical Application on page 1). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 to be around 100kΩ for optimal transient response. R2 is then given by:

$$R_2 = \frac{R_1}{V_{out} / V_{FB} - 1}$$



Inductor Selection

A 4.7μH to 10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L = \frac{V_{out} \times (V_{in} - V_{out})}{V_{in} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current, 2A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Output Capacitor Selection

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times \left[R_{ESR} + \frac{1}{8 \times f_S \times C_2}\right]$$

Where L is the inductor value and RESR is the equivalent series resistance (ESR) value of the output capacitor. In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L \times C_2} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The STI348X can be optimized for a wide range of capacitance and ESR values.

Layout Consideration

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines and take Figure 4 for reference.

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.

2) Bypass ceramic capacitors are suggested to be put close to the Vin Pin.

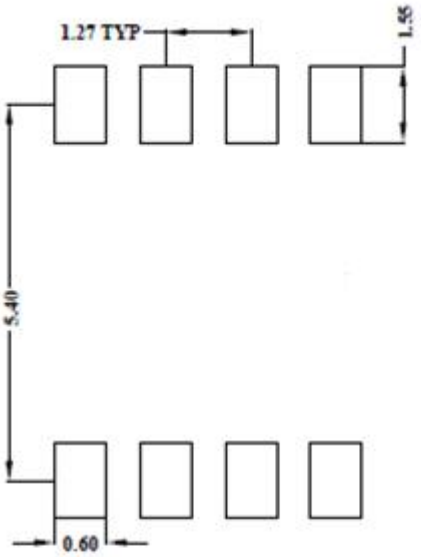
3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) VOUT, SW away from sensitive analog areas such as FB.

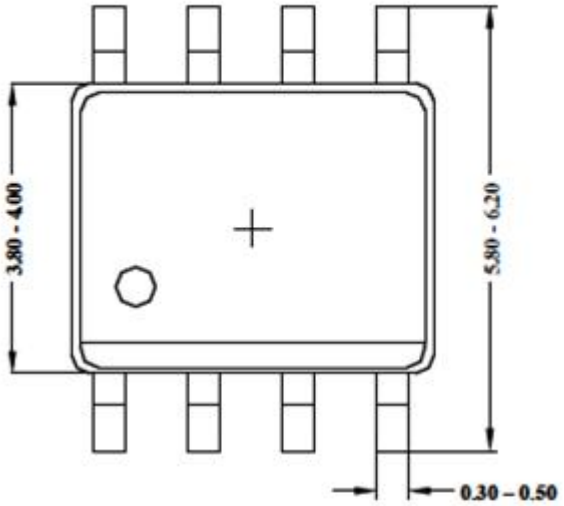
5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

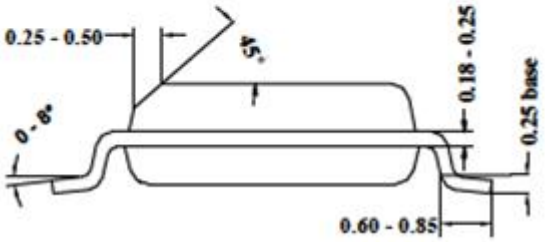
6) An example of 2-layer PCB layout is shown in Figure 4 for reference.

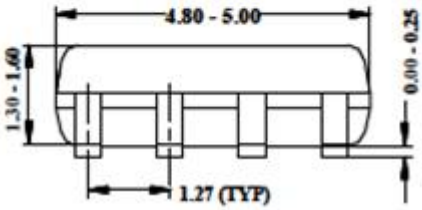
PACKAGE INFORMATION



Recommended Pad Layout







SOP8

Note:

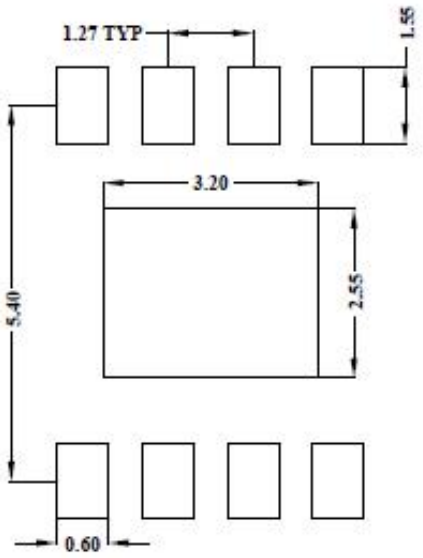
1) All dimensions are in millimeters.

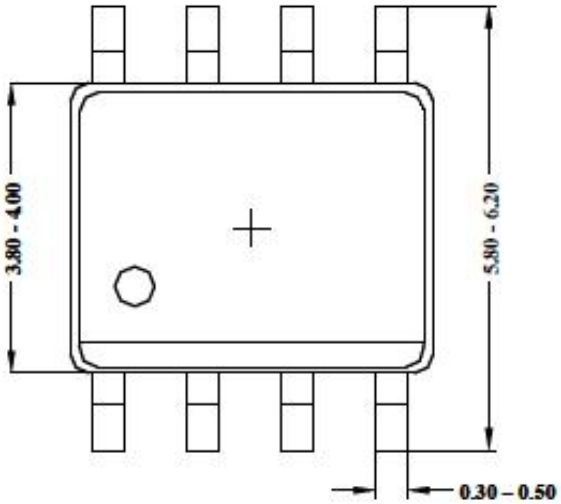
2) Package length does not include mold flash, protrusion or gate burr.

3) Package width does not include inter lead flash or protrusion.

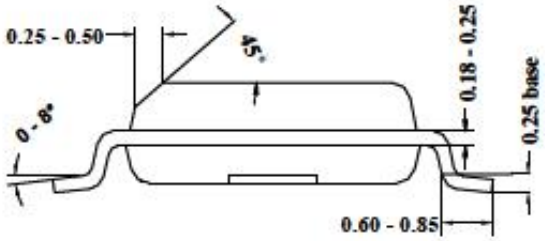
4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.

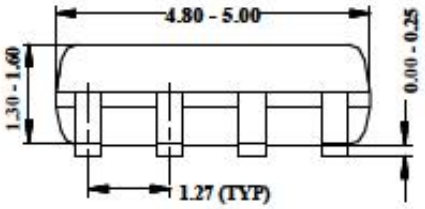
5) Pin 1 is lower left pin when reading top mark from left to right





Recommended Pad Layout





ESOP8

Note:

1) All dimensions are in millimeters.

2) Package length does not include mold flash, protrusion or gate burr.

3) Package width does not include inter lead flash or protrusion.

4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.

5) Pin 1 is lower left pin when reading top mark from left to right