SGM8909
3Vrms Audio Line Driver with Integrated Filter and Programmable Gain Stage

GENERAL DESCRIPTION

The SGM8909 is a single-ended, 3Vrms stereo audio line driver with integrated audio filter. It can reduce external component count, board space and cost. It is ideal for audio applications where single power supply, size and cost are critical design parameters.

The SGM8909 integrates a charge pump to generate a negative supply rail that provides a clean, pop-free ground-biased output. The SGM8909 is capable of driving 3Vrms into a 600Ω load when V_{CC} is 5V or 30mW into 32Ω headset when V_{CC} is 3.3V. Capless output structure allows the removal of the costly output DC-blocking capacitors.

The device has a gain programming pin. With a single resistor from this pin to ground, device gain can be changed to match the line driver with the codec output level. It also reduces the component count and board space.

The SGM8909 will be in mute status during power-on blanking time. External mute control can take over the mute status before power-on blanking time is over, and the SGM8909 can eliminate power up Click-Pop noise perfectly. With the under-voltage protection (UVP) function, SGM8909 will minimize the turn off Click-Pop noise perfectly.

The SGM8909 has built-in active mute control with more that -90dB attenuation for pop-free mute on/off control.

The SGM8909 is available in Green TSSOP-14 package. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Capless Structure to Eliminates Pop-Clicks and Output DC-Blocking Capacitors**
- **2.8V to 5.5V Supply Voltage**
- **Low Noise, Low THD and Low Crosstalk:**
  - **SNR = 107dB at Gain = -1, 600Ω Load for 5V V_{CC}**
  - **Typical V_N = 8.7μVrms from 20Hz to 20kHz at Gain = -1**
  - **THD+N = 0.007% for 600Ω Load and Gain = -1**
  - **Crosstalk is -87dB at 1kHz**
- **3Vrms Output Voltage into 600Ω Load for 5V V_{CC}**
- **2Vrms Output Voltage into 600Ω Load for 3.3V V_{CC}**
- **Supports 32Ω Headset: 30mW at V_{CC} = 3.3V**
- **Single-Ended Input and Output**
- **Programmable Gain by Single External Resistor**
- **Active Mute with More than -90dB Attenuation**
- **UVP Function to Eliminate Turn Off Click-Pop Noise**
- **Integrated Audio Filter**
- **Adjustable Power-On Blanking Time to Eliminate Turn on Click-Pop Noise**
- **Short-Circuit and Thermal Protection**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in the Green TSSOP-14 Package**

APPLICATIONS

PDP/LCD TV
DVD Players
Mini/Micro Combo Systems
Soundcards

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM8909	TSSOP-14	-40℃ to +85℃	SGM8909YTS14G/TR	SGM8909 YTS14 XXXXX	Tape and Reel, 4000

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range ..... -0.3V to 6V
Input Voltage Range ..... V_{SS} - 0.3V to V_{DD} + 0.3V
$\overline{MUTE}$ to GND ..... -0.3 to V_{DD} + 0.3V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 8000V
MM 300V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 2.8V to 5.5V
Operating Temperature Range ..... -40℃ to +85℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

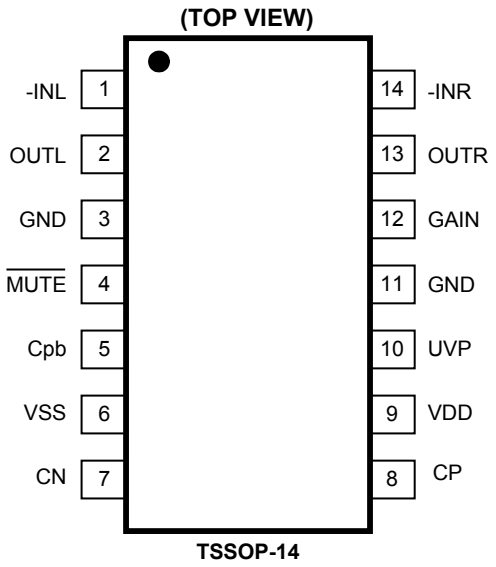
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	FUNCTION
1	-INL	Audio Left Channel Input.
2	OUTL	Audio Left Channel Output.
3, 11	GND	Ground.
4	$\overline{\text{MUTE}}$	Mute Control. Active Low. When $\overline{\text{MUTE}}$ = "Low", chip enters into mute status; when $\overline{\text{MUTE}}$ = "High", chip works normally. There is a 500kΩ pull-low resistor at $\overline{\text{MUTE}}$ pin.
5	Cpb	Power-On Blanking Time Adjusting. Connect one capacitor from Cpb pin to GND to program the power-on blanking time. Chip is in mute status during power-on blanking time.
6	VSS	Charge Pump Output of Negative Power Supply.
7	CN	Charge Pump Flying Capacitor Negative Connection.
8	CP	Charge Pump Flying Capacitor Positive Connection.
9	VDD	Supply Voltage. Connect to positive power supply. When VDD under-voltage event happens, chip will enter into mute status.
10	UVP	Under-Voltage Protection Input. When UVP event happens, chip will be in mute status.
12	GAIN	Gain Programming Pin. Connect a resistor from GAIN pin to GND to program the gain of audio R/L channels.
13	OUTR	Audio Right Channel Output.
14	-INR	Audio Right Channel Input.

TYPICAL APPLICATION

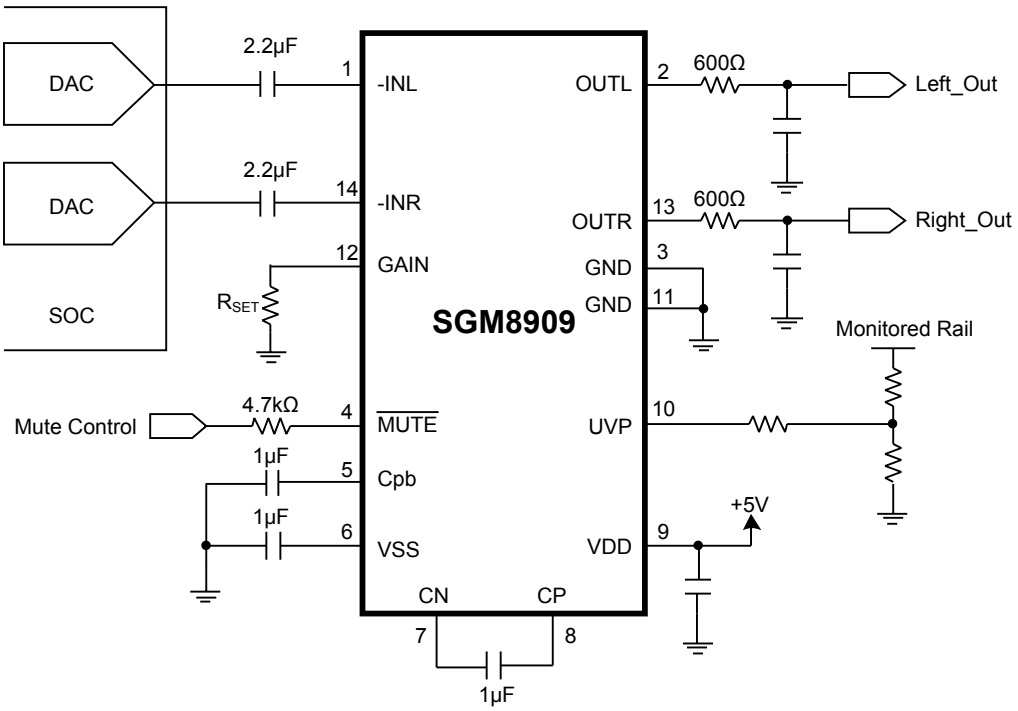


Figure 1. Typical Application Circuit

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, T_A = +25℃, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS (V_{DD} = 3.3V, R_L = 600Ω, C_{PUMP} = 1μF, C_{PVSS} = 1μF, C_{pb} = 1nF)					
Output Offset Voltage ($\|V_{OS}\|$)			1.5	11	mV
Power Supply Rejection Ratio (PSRR)	V_{DD} = 2.8V to 5.5V		-81		dB
High-Level Output Voltage (V_{OH})	V_{DD} = 3.3V, R_L = 600Ω	3.2			V
Low-Level Output Voltage (V_{OL})	V_{DD} = 3.3V, R_L = 600Ω			-3.04	V
External Under-Voltage Detection (V_{UVP})		1.03	1.12	1.23	V
Supply Current (I_{VDD})	$\overline{MUTE}$ = 3.3V, no load		11	14.2	mA
	Shutdown mode, $\overline{MUTE}$ = 0V, no load		3.2	4	
OPERATING CHARACTERISTICS (V_{DD} = 3.3V, Gain = -1, C_{PUMP} = 1μF, C_{PVSS} = 1μF, C_{pb} = 1nF					
Output Voltage, Outputs in Phase (V_O)	f = 1kHz, R_L = 600Ω, THD+N = 1%	2.05			Vrms
Total Harmonic Distortion + Noise (THD+N)	f = 1kHz, BW = 22Hz to 22kHz, R_L = 600Ω, Vo = 2Vrms		0.033		%
	f = 1kHz, BW = 22Hz to 22kHz, R_L = 32Ω, Po = 30mW		0.1		%
Output Power to 32Ω Headset	f = 1kHz, BW = 22Hz to 22kHz, R_L = 32Ω, THD+N = 0.1%		30		mW
Signal to Noise Ratio (SNR)	f = 1kHz, BW = 22Hz to 22kHz, A-weighted, R_L = 600Ω, Vo = 2Vrms		-107		dB
	f = 1kHz, BW = 22Hz to 22kHz, A-weighted, R_L = 32Ω, Po = 30mW		-101		dB
Dynamic Range (DNR)	A-weighted, R_L = 600Ω, Vo = 2Vrms		-75		dB
	A-weighted, R_L = 32Ω, Po = 30mW		-63		dB
Noise Output Voltage (V_N)	A-weighted, BW = 22Hz to 22kHz, f = 1kHz		8.7		μVrms
Input-to-Output Attenuation when Muted	$\overline{MUTE}$ = GND, R_L = 600Ω, f = 1kHz, 2Vrms input		-90		dB
	$\overline{MUTE}$ = GND, R_L = 32Ω, f = 1kHz, 1Vrms input		111		dB
Crosstalk	f = 1kHz, R_L = 600Ω, Vo = 2Vrms		-87		dB
	f = 1kHz, R_L = 32Ω, Po = 30mW		-66		dB
Output Current Limit (I_O)	V_{DD} = 3.3V		83		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, T_A = +25℃, unless otherwise noted)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ELECTRICAL CHARACTERISTICS (V_{DD} = 5V, R_L = 600Ω, C_{PUMP} = 1μF, C_{PVSS} = 1μF, C_{pb} = 1nF)					
Output Offset Voltage ($\|V_{OS}\|$)			1.5	11	mV
High-Level Output Voltage (V_{OH})	V_{DD} = 5V, R_L = 600Ω	4.85			V
Low-Level Output Voltage (V_{OL})	V_{DD} = 5V, R_L = 600Ω			-4.6	V
External Under-Voltage Detection (V_{UVP})		1.03	1.12	1.23	μA
Charge Pump Switching Frequency (f_{CP})		350	470	600	kHz
High-Level Input Current ($\overline{MUTE}$) ($\|I_{IH}\|$)	V_{DD} = 5V, V_I = V_{DD}			1	μA
Low-Level Input Current ($\overline{MUTE}$) ($\|I_{IL}\|$)	V_{DD} = 5V, V_I = 0V			1	μA
External Under-Voltage Detection Hysteresis Current (I_{Hys})			-4.93		μA
Supply Current (I_{VDD})	$\overline{MUTE}$ = 5V, no load		12	15.5	mA
	Shutdown mode, $\overline{MUTE}$ = 0V, no load		3.4	4.1	
OPERATING CHARACTERISTICS (V_{DD} = 5V, Gain = -1, C_{PUMP} = 1μF, C_{PVSS} = 1μF, C_{pb} = 1nF					
Output Voltage, Outputs in Phase (V_O)	f = 1kHz, R_L = 600Ω, THD+N = 1%	3.05			Vrms
Total Harmonic Distortion + Noise (THD+N)	f = 1kHz, BW = 22Hz to 22kHz, R_L = 600Ω, Vo = 2Vrms		0.007		%
	f = 1kHz, BW = 22Hz to 22kHz, R_L = 32Ω, Po = 30mW		0.088		%
Output Power to 32Ω Headset	f=1kHz, BW = 22Hz to 22kHz, R_L = 32Ω, THD+N = 0.1%		34		mW
Signal to Noise Ratio (SNR)	f =1kHz, BW = 22Hz to 22kHz, R_L = 600Ω, A-weighted, V_O = 2Vrms		-107		dB
	f =1kHz, BW = 22Hz to 22kHz, R_L = 32Ω, A-weighted, P_O = 30mW		-101		dB
Dynamic Range (DNR)	A-weighted, R_L = 600Ω, V_O = 2Vrms		-85		dB
	A-weighted, R_L = 32Ω, P_O = 30mW		-64		dB
Noise Output Voltage (V_N)	A-weighted, BW = 22Hz to 22kHz, f = 1kHz		8.7		μVrms
Input-to-Output Attenuation when Muted	$\overline{MUTE}$ = GND, R_L = 600Ω, f = 1kHz, 2Vrms input		-90		dB
	$\overline{MUTE}$ = GND, R_L = 32Ω, f = 1kHz, 1Vrms input		111		dB
Crosstalk	f = 1kHz, R_L = 600Ω, Vo = 2Vrms		-87		dB
	f = 1kHz, R_L = 32Ω, Po = 30mW		-66		dB
Output Current Limit (I_O)	V_{DD} = 5V		142		mA
$\overline{MUTE}$ PIN					
Input High Voltage (V_{INH})		1.5			V
Input Low Voltage (V_{INL})				0.6	V
RECOMMENDED OPERATING CONDITIONS					
DC Supply Voltage (V_{DD})		2.8		5.5	V

PROGRAMMABLE GAIN SETTINGS (1) (2)

(V_{DD} = 3.3V, T_A = +25℃, R_{LOAD} = 10kΩ, C_{CP} = 1μF, Gain = 1, unless otherwise noted)

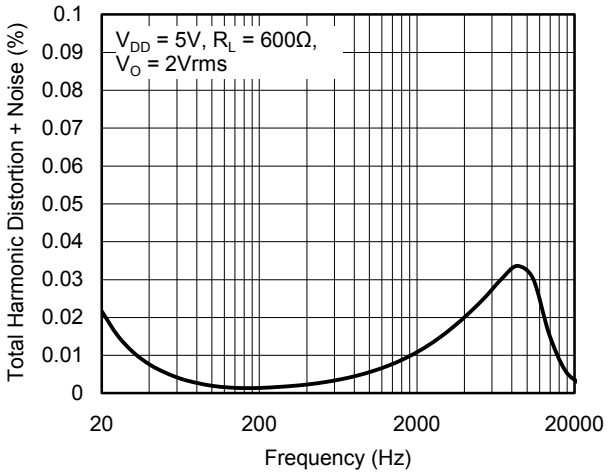
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Programming Resistor Tolerance (R_{TOL})				2	%
Gain Matching (ΔA_V)	Between left and right channels		0.2		dB
Gain Step Tolerance			0.2		dB
Gain Steps	Gain resistor 2% tolerance				V/V
	1000kΩ or higher		-3		
	560kΩ		-1		
	330kΩ		-1.5		
	220kΩ		-2		
	150kΩ		-2.3		
	90.9kΩ		-2.5		
	56kΩ		-3.3		
	39kΩ		-4		
	22kΩ		-5.1		
	15kΩ		-5.5		
	10kΩ		-6.3		
	6.8kΩ		-8.2		
	3.9kΩ		-10		
Input Impedance	Gain resistor 2% tolerance				kΩ
			20		

NOTES:
1. If the GAIN pin is left floating, an internal pull-up sets the gain to -3.
2. Gain setting is latched during power up.

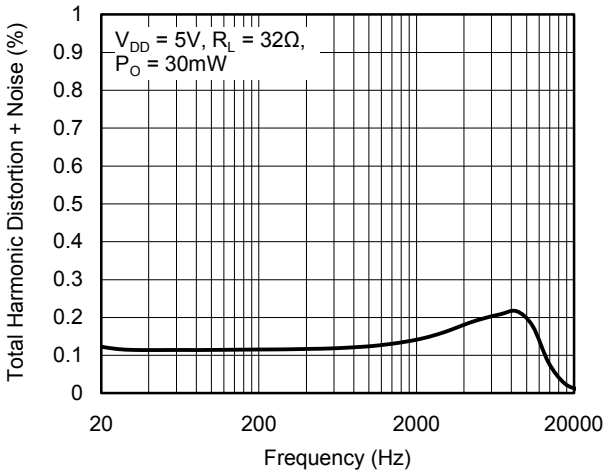
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, T_A = +25℃, C_{PUMP} = C_{PVSS} = 1μF, C_{pb} = 1nF, BW = 22Hz to 22kHz, Gain = -1, unless otherwise noted.

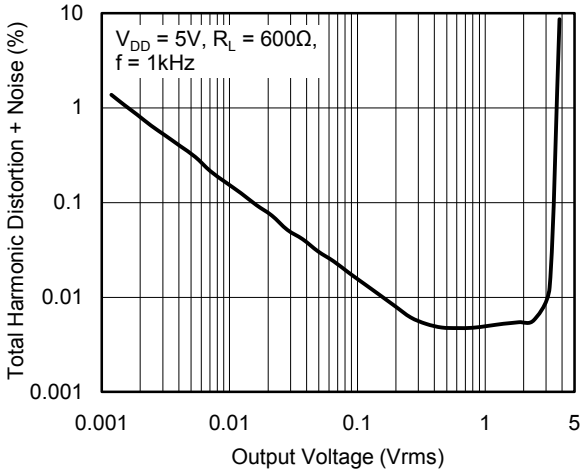
THD+N vs. Frequency



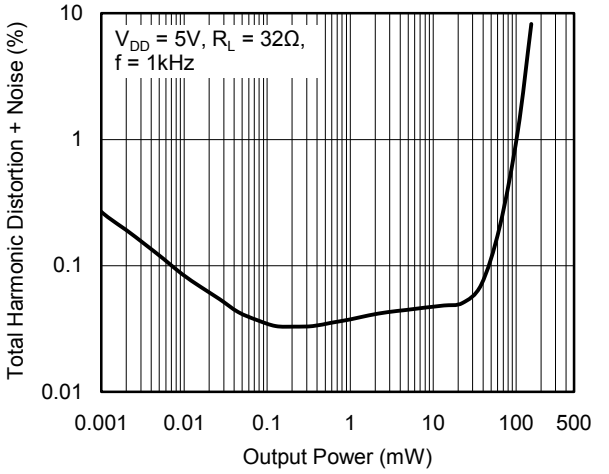
THD+N vs. Frequency



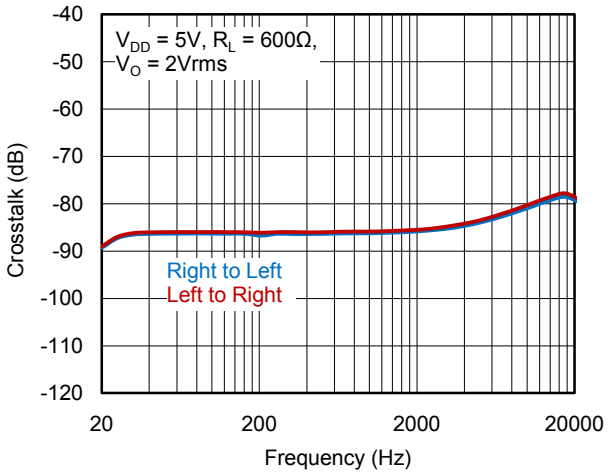
THD+N vs. Output Voltage



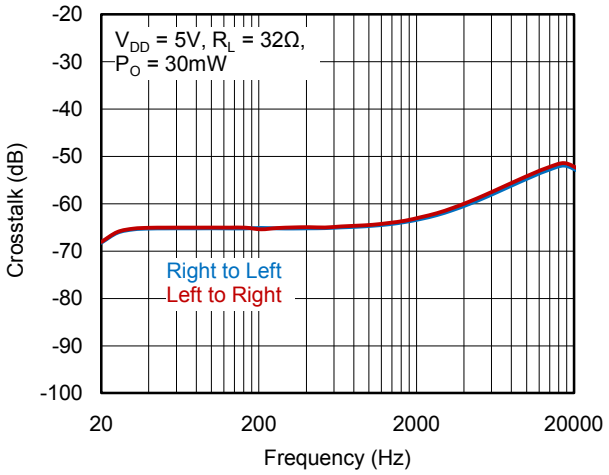
THD+N vs. Output Power



Crosstalk vs. Frequency

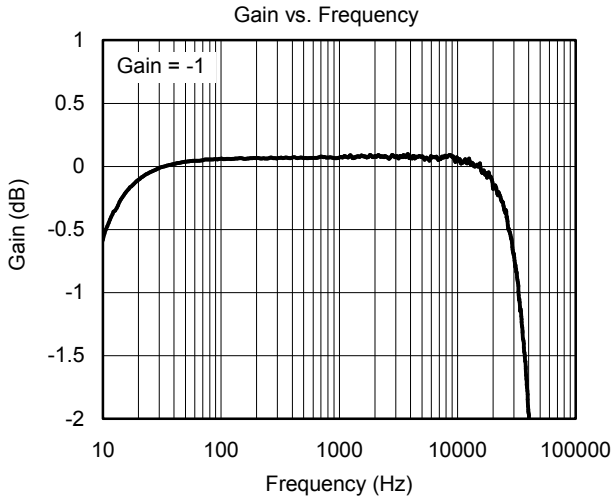


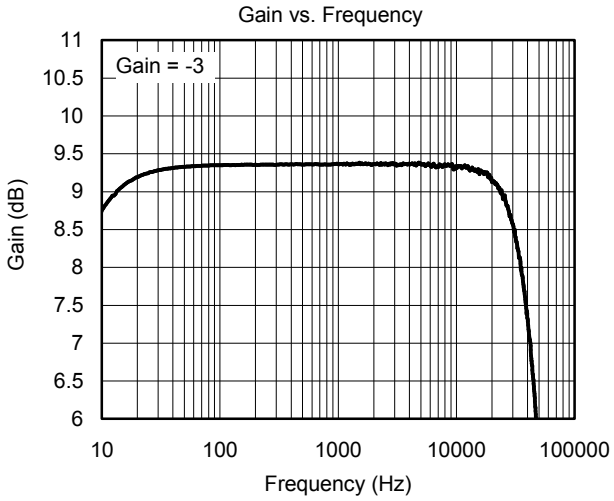
Crosstalk vs. Frequency



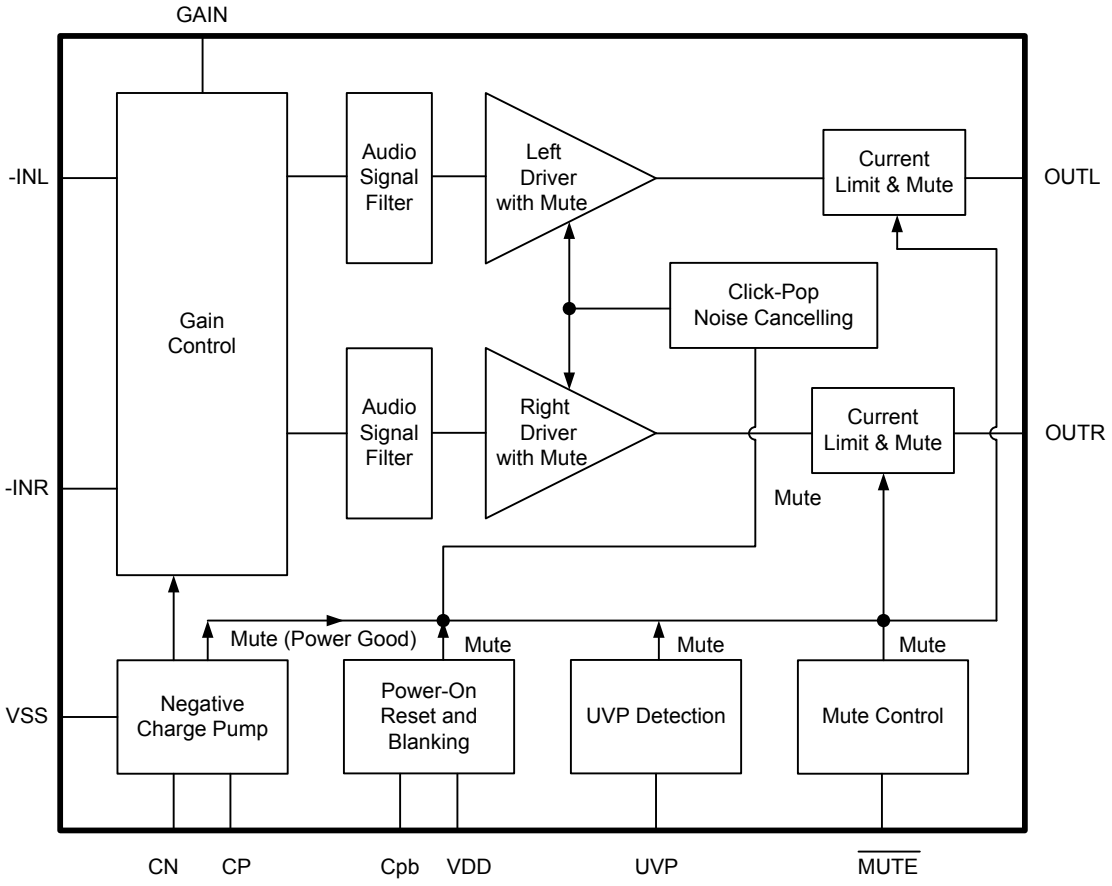
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{DD} = 5V, T_A = +25℃, C_{PUMP} = C_{PVSS} = 1μF, C_{pb} = 1nF, BW = 22Hz to 22kHz, Gain = -1, unless otherwise noted.





SYSTEM BLOCK DIAGRAM



APPLICATION INFORMATION

Single-supply line driver amplifiers typically require DC-blocking capacitors. The top drawing in Figure 2 illustrates the conventional line driver amplifier connection to the load and output signal.

DC-blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

The capless amplifier architecture operates from a single supply but makes use of an internal negative charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volt with the capability to swing to the positive rail or negative rail. Combining this with the built-in click-pop-reduction circuit, the capless amplifier requires no output DC-blocking capacitors. The bottom block diagram and waveform of Figure 2 illustrate the ground-referenced line driver architecture. This is the architecture of the SGM8909.

Charge Pump Flying Capacitor and VSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1μF is typical.

Decoupling Capacitors

The SGM8909 is a capless line driver amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 2.2μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the SGM8909 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

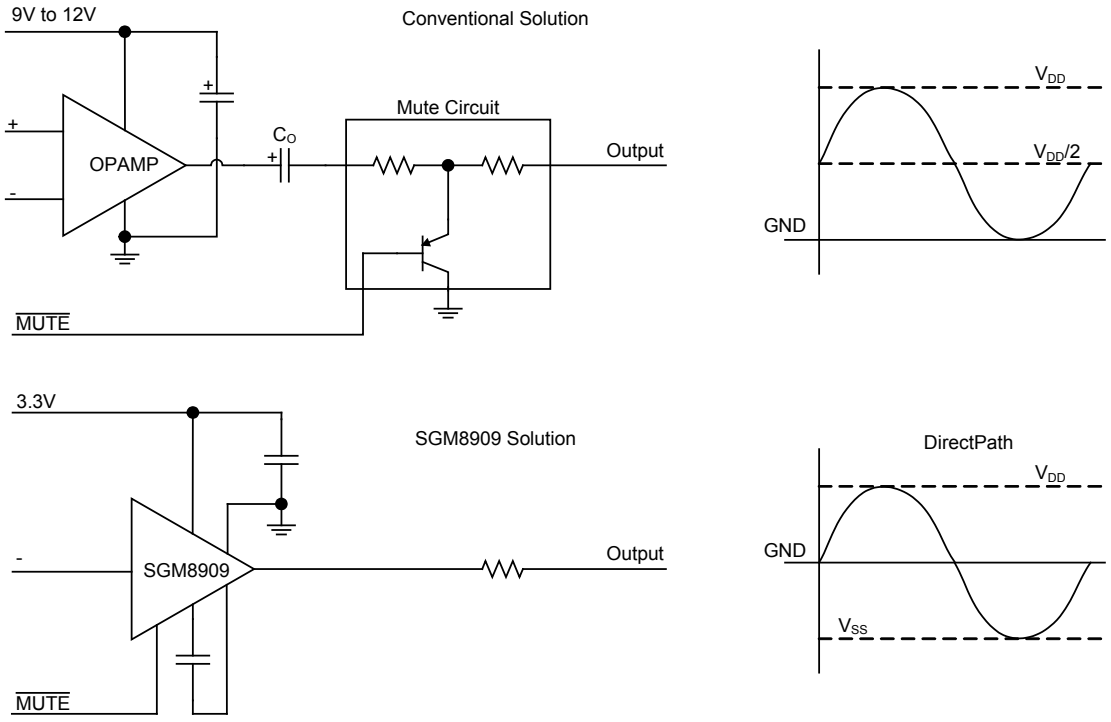


Figure 2. Conventional and Capless Line Driver

APPLICATION INFORMATION (continued)

Gain Setting

The gain setting is programmed with the GAIN pin. Gain setting is latched during power up. Table 1 lists the gain settings.

Table 1. Gain Settings

GAIN SET RESISTOR (kΩ)	GAIN	GAIN (dB)	INPUT RESISTANCE (kΩ)
1000 or higher	-3	9.5	20
560	-1	0.0	20
330	-1.5	3.5	20
220	-2	6	20
150	-2.3	7	20
90.9	-2.5	8	20
56	-3.3	10.4	20
39	-4.0	12	20
22	-5.1	14	20
15	-5.5	14.8	20
10	-6.3	16	20
6.8	-8.2	18.3	20
3.9	-10	20	20

NOTE: If GAIN pin is left unconnected (open), default gain of -3 is selected.

Internal Under-Voltage Detection

The SGM8909 contains an internal precision band-gap reference and a comparator used to monitor the VDD supply voltage and the power rail connected to UVP pin. The internal VDD monitor is set to 2.8V with 200mV hysteresis. When UVP event happens, SGM8909 will enter into mute status.

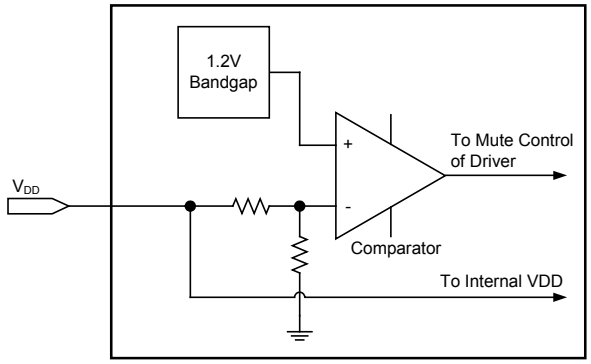


Figure 3. Internal UVP Detection

External Under-Voltage Detection

External under-voltage detection can be used to mute the SGM8909 before an input device can generate a pop.

The threshold seen at the UVP pin is 1.12V. A hysteresis is introduced with a resistive divider, where thresholds for startup and shutdown are determined respectively as follows:

Startup Threshold: $V_{UDPR} = 1.12V \times (R_{11} + R_{12}) / R_{12}$

Shutdown Threshold: $V_{UDPF} = 1.12V \times (R_{11} + R_{12}) / R_{12} - 4.93\mu A \times (R_{13} + R_{11} \parallel R_{12}) \times (R_{11} + R_{12}) / R_{12}$

Hysteresis: $4.93\mu A \times (R_{13} + R_{11} \parallel R_{12}) \times (R_{11} + R_{12}) / R_{12}$

The R_{13} is optional. If the R_{13} is not used, the UVP pin connects to the divider center tap directly.

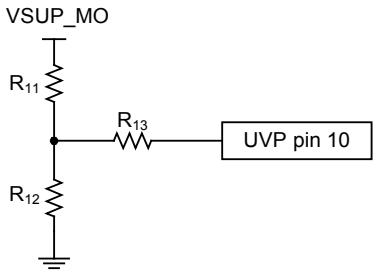


Figure 4. External UVP Setup

Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the SGM8909. These capacitors block the DC portion of the audio source and allow the SGM8909 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1:

$$f_{C_{IN}} = \frac{1}{2\pi R_{IN} C_{IN}} \text{ or } C_{IN} = \frac{1}{2\pi f_{C_{IN}} R_{IN}} \quad (1)$$

APPLICATION INFORMATION (continued)

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ pin low before power-on blanking time is over. The chip should be kept in mute status until the input AC-coupling capacitors are fully charged, this way proper pre-charge of the AC-coupling is performed and pop-less power up is achieved. Figure 5 illustrates the internal circuit and preferred power up sequence.

The power-on blanking time is adjustable. Adjust this time (t_{pb}) by connecting a capacitor (C_{pb}) between Cpb pin and ground. Calculate the external capacitor as follows:

$$C_{pb} = (t_{pb}) / (0.28 \times 10^6) \quad (2)$$

where t_{pb} is in seconds and C_{pb} is in farads.

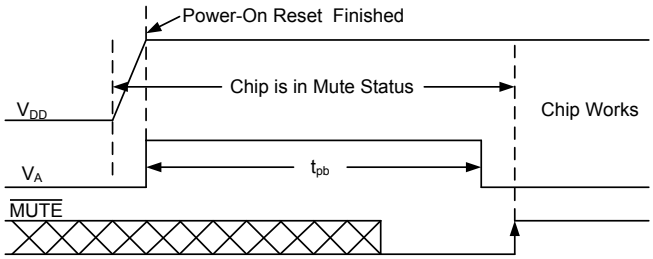


Figure 5. Power Up Sequence

Capacitive Load

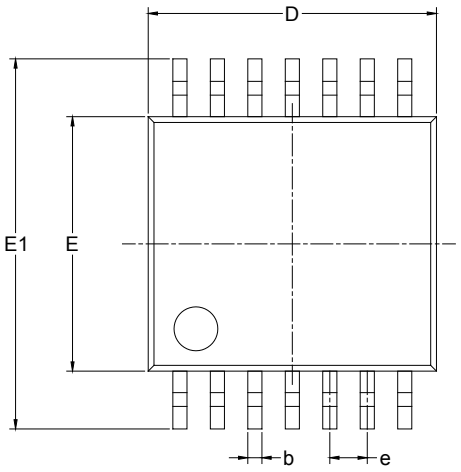
The SGM8909 has the ability to drive a high capacitive load up to 220pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger for the line driver output.

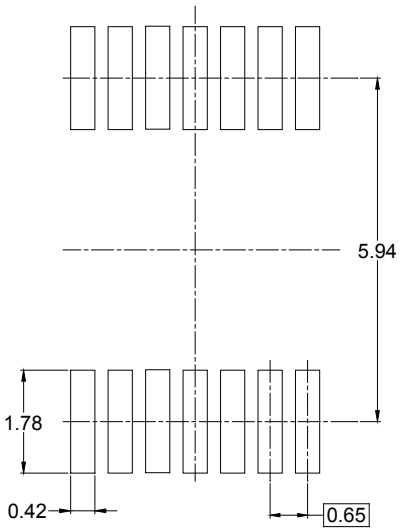
Layout Recommendations

Ground traces are recommended to be routed as a star ground to minimize hum interference. VDD, VSS decoupling capacitors and the charge pump capacitors should be connected with short traces.

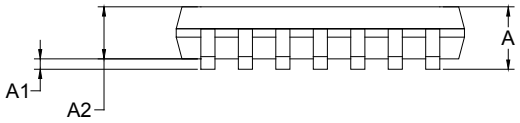
PACKAGE OUTLINE DIMENSIONS

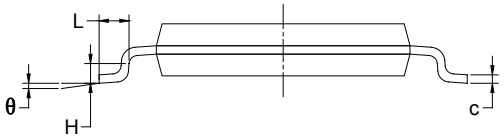
TSSOP-14





RECOMMENDED LAND PATTERN (Unit: mm)

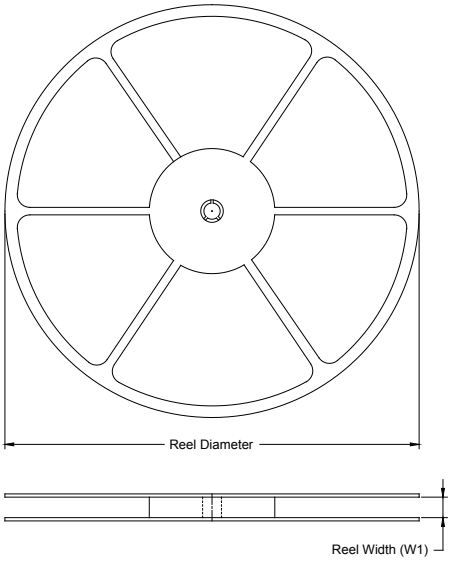




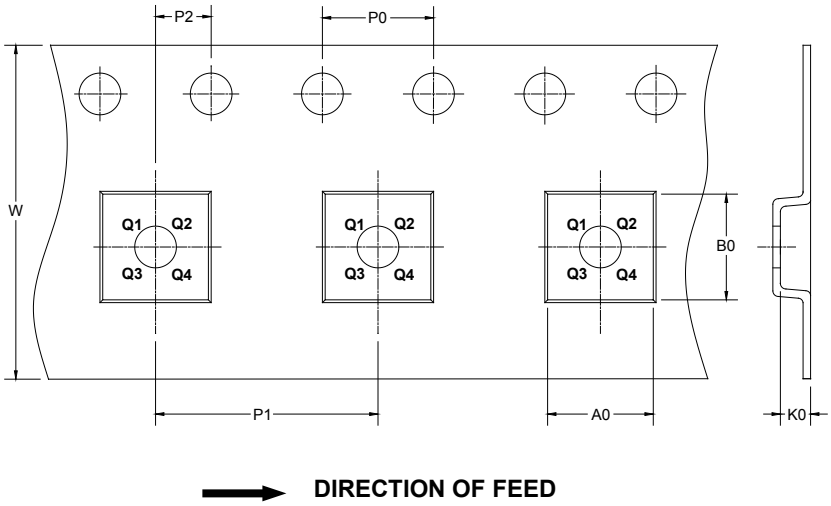
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.860	5.100	0.191	0.201
E	4.300	4.500	0.169	0.177
E1	6.250	6.550	0.246	0.258
e	0.650 BSC		0.026 BSC	
L	0.500	0.700	0.02	0.028
H	0.25 TYP		0.01 TYP	
θ	1°	7°	1°	7°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

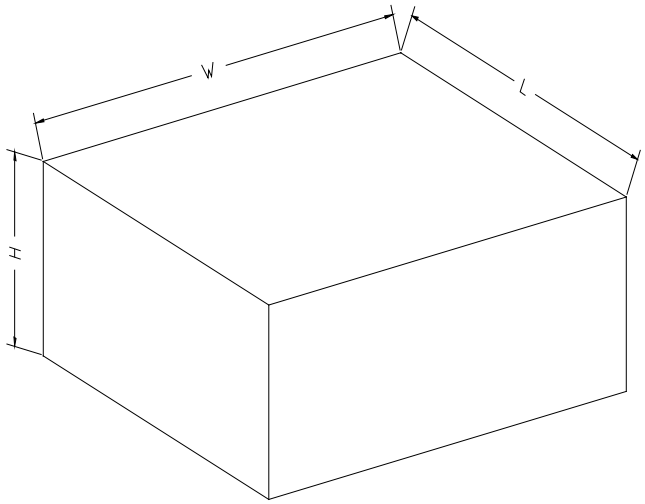
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSSOP-14	13″	12.4	6.95	5.60	1.20	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002